REMARKS

Claims 1-5 are pending.

Claim 1 has been amended to correct several informalities in claim 1 and to address the rejection under 35 U.S.C. § 112, par 2. Applicant respectfully requests withdrawal of those objections and rejections.

The Office action rejected the claims as unpatentable over U.S. 5,835,506 (Kuglin). As discussed below, applicant respectfully request reconsideration.

The claimed subject matter relates to an IC measuring device that determines whether the timing between a data strobe and data from the IC is acceptable. The IC measuring device includes two edge detectors. One edge detector (*e.g.*, E21 in FIG. 1) detects the state of the data strobe, and the second edge detector (*e.g.*, E22) detects the state of the data. A judgment section (*e.g.*, J22) determines whether the timing of the data is acceptable "in reference to the data strobe" based on the states detected by the edge detectors.

The rejection of the claims as unpatentable over the Kuglin patent is misplaced. In particular, as explained below, that patent does not disclose or suggest the claimed "judgment section."

The Kuglin patent discloses an integrated circuit tester 10 (FIG. 1) that includes pin electronics circuits 20, each of which may determine the state of an output signal from a device under test (DUT) 11. Each circuit 20 may compare an output signal from the DUT to high or low logic levels during the test cycle and store data indicating the results of the comparison.

FIG. 2 illustrates details of a pin electronic circuit 20. A timing signal generator 34 generates timing (TIMING) signals that have the same frequency as the cycle (CYC) signal (col. 6, lines 52-60). A compare circuit 36 uses the timing signals as reference signals when sampling the DUT output signals. The compare circuit 36 compares the samples signals to expected values and generates a FAIL signal if the samples do not match the expected values.

FIG. 6 illustrates further details of the compare circuit 36, which can use an edge mode for determining the state of the DUT output signal (col. 11, lines 53-55). Time event generators (TEGs) 84 (*see* upper-right of FIG. 6) receive the TIMING signals from the timing signal generator 34 and produce output strobe pulses STBH, STBL. Those strobe pulses are used by edge comparators 92, 94 (*see* center of FIG. 6) to sample outputs from comparators 86, 88, which compare the DUT output signals to high and low logic levels (VOH, VOL). The edge comparators 92, 94 sample the HIGH and LOW signals from the comparators 86, 88 in response to the STBL and STBH strobe pulses and provide output signals to comparison circuits 102, 104, which compare the actual results to expected results (CM[1:0]). If the actual results do not match the expected results, the comparison circuits 102, 104 generate the FAIL signal.

The STBH and STBL strobe pulses in the Kuglin patent are not generated by the DUT. Therefore, those signals do not correspond to the data strobe signals recited in the pending claims which are outputted <u>from</u> the IC to be measured.

Furthermore, even if one were to assume that the integrated circuit tested 10 of the Kuglin patent could use a first pin electronics circuit 20 to test data strobe signals from the DUT and a second pin electronics circuit 20 to test the data signals from the DUT, there would still be no suggestion in the Kuglin patent of the subject matter of the pending claims. That is because each of the compare circuits 36 would only make a determination regarding signals from a single input/output (I/O) terminal of the DUT. Thus, one compare circuit 36 could check data strobe signals from a first I/O terminal, and a different compare circuit 36 could check data signals from a second I/O terminal. There is no circuitry, however, in the Kuglin patent for determining whether the timing of the data is acceptable with reference to the data strobe as is recited in connection with the "judgment section" of claim 1.

The Office action (at the top of page 5) alleges that Kuglin patent's disclosure of "Multiple pass testing" at col. 2, line 36, somehow would have rendered the claimed subject matter obvious. The applicant respectfully disagrees.

As explained by the Kuglin patent, "multiple pass testing" refers to using all or part of the vector data during two separate phases of the test (col. 2, lines 36-38). One of the main ideas in the Kuglin patent is the capability of the IC tester 10 to operate in either a normal mode or a doublet mode (col. 2, line 62 – col. 3, line 8). When operating in the doublet mode, the pin electronics circuit 20 interprets an incoming vector as defining activities to be carried out during two successive test cycles. Applicant fails to see the relevance of the Kuglin patent's disclosure of the multiple pass testing and how that possibly would have rendered the pending claims obvious.

In view of the foregoing remarks, applicant submits that the pending claims are patenably distinct over the Kuglin patent.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

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Respectfully submitted,

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